WHAT IS CLAIMED IS:

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1. A semiconductor chip package comprising:

a substrate having a plurality of bonding pads;

a semiconductor chip having a plurality of conductive bumps on a front side thereof, the conductive bumps contacting the bonding pads;

a heat slug bonded to a backside of the semiconductor chip; and

a solder film that bonds the heat slug to the backside of the semiconductor chip..

2. The semiconductor chip package of claim 1, wherein the solder film includes one selected from a group consisting of Pb, Sn, Ag, In, and Bi.

3. The semiconductor chip package of claim 1 wherein the backside of the semiconductor chip includes a metal layer formed thereon for strengthening the adhesion between the semiconductor chip and the metal film.

4. The semiconductor chip package of claim 3 wherein the metal layer is a multi-layered film selected from a group consisting of VNi/Au, Ti/VNi/Au, Cr/VNi/Au, Ti/Pt/Au, Cr/CrCu/(Cu)/Au, TiW/(Cu, NiV)/Au, VNi/Pd, Ti/VNi/Pd, Cr/VNi/Pd, Ti/Pt/Pd, Cr/CrCu/(Cu)/Pd and TiW/(Cu, NiV)/Pd.

5. The semiconductor chip package of claim 1, wherein a space between the semiconductor chip and the substrate is filled with an underfilling material.

6. The semiconductor chip package of claim 1, wherein the solder film has a size equal to or lager than a size of the semiconductor chip.

7. The semiconductor chip package of claim 1, wherein the heat slug is formed of a material selected from a group consisting of Cu, Al, and CuW.

8. The semiconductor chip package of claim 1, wherein the heat slug comprises an adhesion layer formed on a surface of the heat slug that contacts the solder film.

9. The semiconductor chip package of claim 8, wherein the adhesion layer is a layer selected from a group consisting of a Ni/Au layer, a Ag layer, and a Pd layer.

10. The semiconductor chip package of claim 1, wherein the heat slug is coated with an anodizing layer.

11. The semiconductor chip package of claim 1, wherein the heat slug is shaped such that a portion of the heat slug is attached to the substrate by an adhesive..

12 The semiconductor chip package of claim 11, wherein the adhesive includes silicon rubber or elastomer.

13. The semiconductor chip package of claim 1, wherein a plurality of throughholes are formed on the heat slug.

14. A method of fabricating a semiconductor chip package, comprising:

preparing the semiconductor chip having a plurality of conductive bumps on a front surface of the semiconductor chip;

bonding a heat slug on a backside of the semiconductor chip using a solder film; and

attaching the semiconductor chip on a substrate such that the conductive bumps of the semiconductor chip contacts a plurality o bonding pads on the substrate.

15. The method of claim 14, further comprising filling a space between the semiconductor chip and the substrate.

16. A semiconductor chip package comprising:

a substrate having a plurality of bonding pads;

a semiconductor chip having a plurality of conductive bumps on a front side thereof, the conductive bumps contacting the bonding pads;

a heat slug bonded to a backside of the semiconductor chip, the heat slug comprising a top portion, side standing portions bent from the top portion, and side end portions bent again from the side standing portions; and

a solder film that bonds the heat slug to the backside of the semiconductor chip;

wherein the top portion of the heat slug contacts the conductive solder film and the side end portions of the heat slug are attached to the substrate by an adhesive.

17. The semiconductor chip package of claim 16, wherein the solder film has a size equal to or larger than a size of the semiconductor chip.

18. The semiconductor chip package of claim 16, wherein the heat slug is formed of a material selected from a group consisting of Cu, Al, and CuW.

19. The semiconductor chip package of claim 16, wherein the heat slug comprises an adhesion layer formed on a surface of the heat slug that contacts the solder film.

20. The semiconductor chip package of claim 16, wherein the heat slug is coated with an anodizing layer.